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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

J. P. KOTOWSKI, ET AL.

Application No. 10/067,441

Filed: February 4, 2002

For: **INTEGRATED CIRCUIT AND METHOD FOR TESTING SAME USING SINGLE PIN TO CONTROL TEST MODE AND NORMAL MODE OPERATION**

Group Art Unit: 2824

Examiner: JUNG H. HUR

RESPONSE TO OFFICE ACTION MAILED ON APRIL 23, 2003

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on June 18, 2003.

GIRARD & EQUITZ LLP Date: 06/18/03

By: Marsha A. Townsend

Marsha A. Townsend

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Office Action mailed April 23, 2003, in the referenced application. Please enter the following amendment and consider the following remarks.

IN THE ABSTRACT:

Amend the abstract to read as follows [attached is an appendix including a marked up version of the amended abstract showing the differences between the text as originally filed and as hereby amended]:

An integrated circuit including operational circuitry operable in response to at least one control signal asserted to an external node from an external source, and test circuitry coupled to the external node and the operational circuitry. In response to data asserted to the external node from an external source, the test circuitry enters a test mode in which it tests, configures, or reconfigures the operational circuitry. The test circuitry also asserts to the operational circuitry each control signal received at the external node (or an amplified or